AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 9, line 24 as follows:

The Pulse Generator Buffer (PGB) 58 works in conjunction with the SRVG/TM 28 of the PVGA 12. The Timer Module portion of the SRVG/TM 28 can produce a wide range of clock signals based on either its local fixed oscillator or the programmable clock from the DTB 34. In addition, the video portion of the SRVG/TM 28 can produce arbitrary complex digital patterns. These digital signals may be in ~~TTL~~ transistor-transistor logic (TTL) form. The PGB 58 in the SC/SD 14 will accept the TTL level inputs and level shift them to user-specified voltages. The output buffer will provide high current output drive and impedance matching. With the SC/SD 14 including emulators DME 52, CTE 54 and DOE 56, input signals from the UUT 24, which are in a form unprocessable by the PVGA 12, are converted into a form processable by the PVGA 12. On the same token, in view of the bi-directional signal transfer between the SC/SD 14 and the UUT 24 and between the PVGA 12 and the SC/SD 14 (see FIG. 3), the emulators also convert output signals from the PVGA 12, which are in a form unprocessable by the UUT 24, into a form processable thereby.